Name: SAIF NAJIM ISMAIL

Contact:

Address: District College of Agriculture old location 8666 +JJ3, Abu Ghraib, Baghdad, 10081, Iraq

Email: sai91f@gmail.com

Expertise:

- FPGA Design Altera Quartus
- HDL (VHDL & Verilog)
- Synthesis/Implementation
- RTL Design
- Timing Analysis
- Board Design
- Simulation/Testing
- Embedded Systems
- SoC Design
- Debugging/Troubleshooting
- Bash Scripting,C&C++,C#, Python
- MATLAB and AutoCAD

Main Field of Research:

- Custom Architectural
- Design of Embedded System
- Digital Signal processing (DSP)
- Parallel Structures
- Parallelism (spatial and temporal)
- Pipeline Processing
- Design of Computer Engine
- Data processing

Language:

Language	Speaking	Listening	Writing
English	Excellent	Excellent	Excellent
Malay	Basic	Basic	Basic
Arabic	Native Language		

FPGA Hardware Design Engineering

I am excited to get an opportunity for the FPGA or engineer position at designer electronics. Currently, I have a PhD degree in Computer Engineering (Hardware) and seven years of experience in the Academic Field. I possessed excellent interpersonal skills, I am determined, creative and good in decision making and interacting with people at all levels. I am confident that I have the skills and experience looking for and would be a valuable addition to company team.

Experience Academic Education

2023 | Malaysia-Perlis **(UniMAP)** | Currently (Postdoctoral) (Remote)

Performance Analysis of Different FPGA Architectures for High Throughput Computing Engine Based on VLC Communication Transceiver

2018 - 2023 | Perlis-Malaysia
University Malaysia Perlis (**UniMAP**) | PhD. Computer Eng. (Hardware Design)
The PhD Study was a Research Mode
Thesis Title | Supervisor (Prof. Madya Ir. Dr. Mohd Rashidi Che Beson)

Design and Implementation of Embedded Multiple Engine FPGA-based Visible Light Communication Transceiver

This thesis describes the architectural design and implementation of embedded multiple (quad) computing engines in FPGA based visible light communication (VLC) transceivers. The proposed approach for computing engines consisted of three main parts, namely the UART, FIFO buffer, and 128-bit AES algorithm.

2016-2017 | Perlis-Malaysia
University Malaysia Perlis (**UniMAP**) | MSc. Embedded System Design Eng.

The Master Study was a Mixed Mode, and my CGPA = 3.16 / 4.00
Thesis Title | Supervisor (Dr. MUATAZ HAMEED SALIH AL-DOORI)

Design and Implementation of Embedded Vision Based Tracking system using FPGA-SoC

In this project of object tracking is a fundamental component of embedded vision that is very beneficial in several applications such as unmanned vehicles, surveillance, automated traffic control, biomedical image analysis and intelligent robots. The proposed method has adopted a passive tracking vision system based on platform DE1-SoC and D5M camera. Every frame captured by the camera is processed to detect the targeted object using a colour based approach.

2010 - 2014 | Baghdad-Iraq

University Al Salam college| B.Sc Computer Technology Eng.

Grade = 66.6 % (My rank was the 27st out of 133 graduates)

International Conferences: Technical Committee

Position	Conference
Technical Committee	2nd International Conference on Materials Engineering and Science (IConMEAS 2019), 25-26/September/2019, University of Technology, Baghdad – Iraq
Technical Committee	3nd International Conference on Materials Engineering and Science (IConMEAS 2020), 28-30/December/2020, Kuala Lumpur, Malaysia
Technical Committee	4nd International Conference on Materials Engineering and Science (IConMEAS 2021), 06-07/October/2021, Duhok, Kurdistan Region, Iraq
Technical Committee	5nd International Conference on Materials Engineering and Science (IConMEAS 2022), 22-23/August/2022 University of Technology, Istanbul, Turkey

Reference

Dr. MUATAZ HAMEED SALIH AL-DOORI
Senior Staff Engineer Manager at Flex Company Penang
Phone: +60124619256
Email: muatazhameed@gmail.com

PROF. MADYA Ir. Dr. Mohd Rashidi Che Beson
Lecturer Computer Engineering (UniMap) Perlis
Phone: 04-988-5670
Email: rashidibeson@unimap.edu.my

Soft Skills:

- Time Management
- Teamwork
- Leadership
- Communication
- Critical Thinking
- Solving Problem
- Time Management
- Adaptability
- Leadership
- Creativity
- Organization
- Attention to Detail
- Highly motivated
- Fast learn for technologies
- Easy adapt to environments

Computer Skills:

- MS Office Word
- Excel
- Power Point

Hardware Board used:

- DE1-SoC board
- DE10-Nano board
- DE2-115 board
- 5 Mega Pixel Digital Camera

Micro-Controllers used:

- NodeMCU (ESP8266)
- Cortex-M7 processor
- STM32 board

Micro-Computers used:

- Raspberry Pi

Chip-Set used:

- Cyclone V
- Cyclone III
- Cyclone II
- MAX 10

Sensor used:

- LM393 Light Sensor
- RFID MFRC522 reader

Experience:

2016 - 2023:

Experience in field FPGA development engineer 7 years:

- **Come up with innovative solutions to improve the performance of a system from software, hardware and networking perspectives.**
- **Carry out the project documentation and progress report to the Line manager and project manager.**
- **To work with other team members to provide technical support to customer FPGA logic design architectural base station hardware development project custom computing engine.**
- **Developing technical documentation, standards and procedures debug support for high- level test scripts developed by coworkers work in an expert team of other module.**
- **Developers and software engineers that develop operational software for the test, qualification and hardware verification design, create VHDL and the top level for Altera FPGAs.**
- **Create a simulation environment for VHDL and functional simulation FIFO, protocols like UART, I2C, and SPI.**
- **Knowledge unit of VGA controlling, Algorithmic AES 128-bit, DES 64 bit**
- **Optimizing power of architectural by use of behaviour design spatial and temporal parallelism**
- **Creating simulation, verification environments, validating designs reviewing, enabling processor and platform features FPGA-based tool TimeQuest Timing Analyzer.**
- **Experience with FPGA development, good knowledge of RTL design and simulation.**
- **Experience with hardware system design and debugging of performance the system specific Knowledge & Proficiencies.**
- **Familiar with FPGA design tool Altera Quartus, IP core, etc.**
- **Basic working knowledge of signal integrity to recognize any problems when**
- **debugging.**
- **Ability to quickly pick up and own new concepts to contribute to innovative solutions.**
- **Strong knowledge of complete FPGA/SoC verification flow.**
- **Good and easy to learn any type of sensor.**
- **Passionate, self-motivated with the ability to learn quickly, independently Knowledge of VHDL design and coding skills for synthesizing FPGA designs.**

Reference:

Research Gate: https://www.researchgate.net/profile/Saif-Ismail-2

Google Scholar: https://scholar.google.com/citations?user=vk6cw5IAAAAJ&hl=ar

citation=33

h-index= 2

https://www.linkedin.com/in/saif-najim-8475b7111/

WORKING EXPERIENCE:

Employer's Name and Address	Position	Date From - to	Employment Status
Academic			
Dr. MUATAZ HAMEED SALIH AL-DOORI Faculty of Electronic Engineering & Technology (FKTEN) UniMAP	Research Assistant (RA)	30/06/2017 - 31/12/2017	Part time

SUPERVISION - MASTER STUDENTS MENTORING:

No.	Name	Project Title	Status
1	Khaldoon Ibrahim Khaleel	An Enhancement of Text to Speech (TTS) System using Raspberry Pi	Graduated 2019
2	Mohammed Ahmed Salman	Design And Implementation Of FPGA Iot-Based Face Recognition System Using Spatial Parallelism	Graduated 2020
3	Husham Ibmhim Mahdi Al Salman	Design and Implementation of Parallel Model Embedded FPGA-Based Computing Architecture for DES Algorithm	Graduated 2022

SELECTED PUBLISHED RESEARCH ARTICLES:

1. Saif N. Ismail, Muataz H. Salih and Wahab Y (2018) "FPGA IMPLEMENTATION OF EMBEDDED COLOR BASED TRACKING SYSTEM FOR SINGLE OBJECT" ARPN Journal of Engineering and Applied Sciences, VOL. 13, NO. 4. ARPN Publishing. (SCOPUS Index).
2. Saif N. Ismail, Muataz H. Salih, Mohammad F. Bin Baharudin (2019) "DESIGN AND IMPLEMENTATION OF FPGA-BASED VISIBLE LIGHT COMMUNICATION" ARPN Journal of Engineering and Applied Sciences, VOL. 14, NO. 2, 455-469 ARPN Publishing. (SCOPUS Index).
3. Salih, M. H., Teng, L. H., & Ismail, S. (2019). Indoor tracking personnel for RFID with FPGA. ARPN J. Eng. Appl. Sci, 14, 439-454. ARPN Publishing. (SCOPUS Index).
4. Salih, M. H., Teng, L. H., & Ismail, S. N. (2019). Design and implementation of tracking personnel within building featuring FPGA and RFID. ARPN J. Eng. Appl. Sci., 14(3), 758-774. ARPN Publishing. (SCOPUS Index).
5. Ismail, S. N., Salih, M. H., & Wahab, Y. (2018). Design and implementation of embedded Tracking system for multiple objects using fpga-soc. ARPN Journal of Engineering Applied Sciences, 13(3), 1085-1097. ARPN Publishing. (SCOPUS Index).
6. Ismail, S. N., & Salih, M. H. (2020, March). A review of visible light communication (VLC) technology. In AIP Conference Proceedings (Vol. 2213, No. 1, p. 020289). AIP Publishing LLC. (SCOPUS Index).
7. Saif N. Ismail, C. B. M. Rashidi, Muataz H. Salih, and N Mahrom (2023) "Design and Implementation of FPGA based Single Computing Engine of VLC Text Transfer" AIP Publishing (SCOPUS Index) (UNDER REVIEW RESEARCH)
8. Saif N. Ismail, C. B. M. Rashidi, Muataz H. Salih, and N Mahrom (2023) "Design and Implementation of FPGA Based Single Computing Engine of VLC Image Transfer" AIP Publishing (SCOPUS Index) (UNDER REVIEW RESEARCH)
9. Saif N. Ismail, Muhmmad Imran Ahmad, Noor Aldeen A.Khalid, Naseer A.ali , Zainab K.fadhil, 'High-Throughput of Processor using Dual Computing Engine of VLC System for Text Transfer Based on FPGA', Bulletin of Electrical Engineering and Informatics (SCOPUS Index) (UNDER REVIEW RESEARCH).

Declaration:

"I hereby declare that the above mentioned information is true to the best of my knowledge".

Dr. SAIF NAJIM ISMAIL