Computer Aided Design, Simulation and Implementation of Multi Switched Mode Power Supplies (SMPS) Controlled by One Microprocessor

Kader H.A. Al-Shara[1], Ahmed Q.A. Al- Oraibi[2]

[1]Al-Farabi University College, Baghdad

[2]Al-Nahrain University Engineering College, Baghdad

Email: Kaderalshara@yahoo.com

Abstract: In this paper an approach of computer design, simulation and implementation of multi switched mode power supplies (SMPS) controlled by one microprocessor is investigated. The design of three switch mode power supplies based on flyback DC-DC converters with different power 20,24 and 6 Watt and output voltages rated +5V,+12V/ and -12V are achieved. The design power stage is based on the bipolar as the main switching device with protection network used to ensure safe operation. The microprocessor and its supervisory board are used with slight software program to control the output of the multi switched mode power supplies (SMPS) even though they have different switching frequency, output voltage, output power. The system performance is simulated and examined under many desired conditions. From the obtained result it was found that, it is efficiently and easily to use one microprocessor to control of multi switched mode power supplies reducing the complexity of the system.

Keywords – SMPS, Fly back, Power Supply, Microprocessor.

1. Introduction

In the recent years, the development of microprocessor and semiconductor memory has produced a generation of electronics system designs which are compact, lightweight, efficient and low cost, following advances in semiconductors, control circuit and passive component, the switching power supply has been mass-product with increasing reliability and cost- effective pricing. The field of power electronics has opened a whole new technology and new dimensions in the world of electronics [1]. The rapid advance in the microelectronics technology and availability of fast and low-cost microprocessors have led to the increasing use of microcomputers in every field of engineering including power electronics. The microprocessor is now regarded as a standard component in power electronics equipment [2], and considerable attention is being paid to the digital control of variable speed drive systems using powerful data processing capabilities of microprocessors. The switching mode power supply (SMPS) becomes a common form of generating the required voltages. Now that reliable high voltage power transistors and control integrated circuits are available at economical prices, the complexity of the switching mode, with respect to the conventional series regulator power supply, can be allowed in order to obtain its major advantages, high efficiency, small size and weight. Further features which add to its usefulness are the ability to regulate over a large range of input voltages, and ease of isolation and provision of a number of voltage supplies. The convergence of recent developments in high-voltage transistors, integrated circuits, and ferrite materials makes the consideration of such supplies more interesting [3], [4].Nowadays Computer Aided Design (CAD) and Computer Simulation are dominant in the analysis and Design of Switching mode power supplies.

A vast amount of technology in the area of switching power supplies modeling, analysis, and control design has been generated in the past four decades. The major goal of the analysis and modeling is to achieve the optimum design of the converter power stage and then reach the most convent controlling method to achieve a stable converter [5].

In case of Flyback converter topology, converter stores the energy when the switch is on and delivers energy to the load when the switch is off. This eliminates the need of additional inductor for storage of energy unlike in the case of forward, half bridge and full bridge topologies. Thus it makes the topology simpler and economical. Flyback converter can be designed to obtain single output and multiple outputs. The detailed analysis of single output, multiple output Flyback converters are provided [6-9].

2. Microprocessor System Supervisor and Controller

Using the microprocessor as a system supervisor and controller is attractive because it greatly reduces the number of components used in the system. In a well-designed microprocessor based system software is used to replace as much hardware as possible causing the complexity of the system to be reduced. Since the characteristics of the system can be changed by simply varying the software, then implementing as many functions as possible in software. This highly increases the flexibility of the system. Those features provide the microprocessor based system with

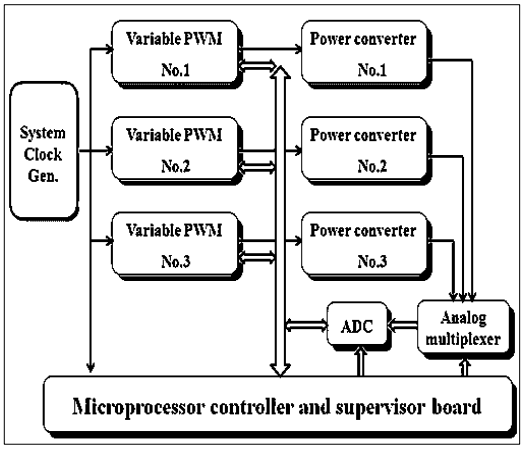

Fig. (1): The basic block diagram of three SMPS's controlled by one microprocessor.

An enhanced ability over the ordinary discreet logic designs [10]. For simple tasks, the microprocessor may be not efficiently to use, while in complex tasks it is so useful, such as using microprocessor controller with one SMPS and using it with multi- SMPS's that means using one microprocessor to control multi- SMPS's is the main advantage from this project. [10].

The microprocessor selects one of the converter output voltages to be inputted to the ADC analogue input. The ADC converts this voltage to an 8-Bit digital data. The microprocessor reads this byte and then read a byte from one of the voltage selection units which represents the desired (or the needed) output voltage level of the selected converter. According to the difference between these two bytes the microprocessor might decide to update the duty cycle of that converter by reprogramming the variable width pulse generator with a new byte. Fig. (1) Shows a basic block diagram of three-switched mode power supplies controlled by one microprocessor which is designed in this paper.

3. Computer Aided- Design (CAD)

Instead of using hand calculations and several trial combinations to select elements of dc.-dc. Converter, CAD leads us to choose the optimum selection of all parameters with minimum effort. In this system, there are three SMPS's with different specifications such as different output voltage, different load current and different input power. The computer program determines the components value as filter capacitor, semiconductor elements and winding wire size. These values are depending upon the equations specifying the system elements accomplished by design limitation as conditions and designer decision. The moderate computer-aided-design program can enable unskilled operator to choose and design the switching regulator that is best adapted to his particular problem. However the operator plays a major role in optimizing the cost and size of the converter. The operator can change some of the specifications or component

selection to overcome contradictions and to optimize the design. The three SMPS's in this paper are all based on flyback dc-dc converter, so that the program contains the equations concerned with the fly back converter.

4. Design Equations

The necessary equations are given to design a flyback converter transformer-choke, and the necessary limitations for the elements used are stated to decide the proper elements types. The design equations are derived for a complete energy transfer mode (i.e. discontinuous inductor current mode). In incomplete (continuous mode) energy transfer, transformer-choke design follows the basic steps given below with some minor changes in the definition of peak collector current (primary current) [2].A variable output voltage d.c. power supply is to be designed here (i.e. output voltage range is $V_{omin.}$ to $V_{omax.}$). The designed power supply may accept an input d.c. voltage in the range of is $V_{imin.}$ to$V_{imax.}$In the flyback converter, regulation is accomplished by varying the duty cycle of the switch through predetermined limits, which are designed as $D_{min.}$ And D_{max},here D_{max} is assumed to have the value of 0.45 (i.e. 45% of the full cycle),this is to keep the duty cycle below (0.5 or 50%),that is to avoid core saturation [5,11].To decide the value of $D_{min.}$, first the minimum duty cycle for maximum output voltage (D_{min*}) will be defined and determined. This duty cycle can be calculated from $D_{max.}$,$V_{imin.}$ And V_{imax},as follows [2].

$$D_{min*}=\frac{Dmax}{(1-Dmax)\left(\frac{Vimax}{Vimin}\right)+Dmax} \quad \ldots\ldots (1)$$

$D_{min.}$is determined when the input voltage is $V_{imax.}$ And the output voltage is $V_{omax.}$ Since the output voltage is directly proportional to the duty cycle, then when the output voltage is needed to be decreased, the duty cycle must be reduce in the same ratio, for example when the output voltage is to be halved, the duty cycle must be halved-and so on. Therefore,

$$D_{min}=D_{min*}.\frac{v_{omin}}{v_{omax}}\ldots\ldots (2)$$

Using this value with the switching frequency, the switching times for the transistor and diodes are determined. It is necessary to determine the transformer peak primary current, which equals the transistor peak collector current.

In the complete energy transfer mode, the current rises up from zero to peak current during the time at which the transistor is ON. At the end of the ON time, the peak primary current is achieved (i.e. to accomplish the peak primary then $V_{in} = V_{imin}$ and the time of ON state = (D_{max}/f).

Hence,

$$I_{pp}=\frac{Vimin.Dmax}{f.L}\text{------ (3)}$$

The output power in the complete energy transfer is equal to the energy stored per cycle times the switching frequency [1].

Since $P_{out} = 1/2\ L.I_{pp}^2.f$ then

$$I_{pp}^2=\frac{2P_{out}}{L.f}\text{------- (4)}$$

Substituting Left from equation (3) in equation (4) yields:

$$I_{pp}=\frac{2Pout}{Vimin.Dmax}\text{------ (5)}$$

From equation (3), the primary inductance can be determined now.

$$L=\frac{Vimin.Dmax}{Ipp.f}\text{------ (6)}$$

To achieve this inductance value, an air gap is introduced in the flux path flatten the hysteresis loop, thus lowering the working flux density [2, 11]. Most of the stored energy in the primary inductance is in the air gap volume v_g since the air gappresents the largest magnetic reluctance in the flux path. Therefore:

$$\frac{1}{2}L.I_{pp}^2=\frac{1}{2}B_{max}.H.v_g\text{------ (7)}$$

Where $v_g = L_gA_e$(L_g: gap length, A_e: the effective cross section area of the core)

Since $\mu_o . \mu_r . H = B_{max}$

$$L_g = \frac{4.\pi.L.Ipp^2 \times 10^{-7}}{Bmax^2.Ae} \text{------- (8)}$$

The magnetic field strength in the gap generated by the primary winding Np can be written as $H = N_p I_{pp} / L_g$

$$N_p = \frac{H.Ig}{Ipp} = \frac{Bmax.Lg}{4.\pi.10^{-7}.Ipp} \text{------- (9)}$$

Then To calculate the secondary winding number or turns, the secondary voltage must be calculated when the input voltage is at its minimum V_{imin}. And the output voltage is at its maximum V_{omax} with maximum duty cycle then [7]:

$$Ns = \frac{Np(V_{omax}+V_D)(1-D_{max})}{V_{imax}.D_{max}} \text{------ (10)}$$

Since the value of the output voltage ripple is inversely proportional to the value of the output capacitor, care must be taken in choosing the value of the capacitor. Large capacitance value causes fewer ripples in the output but greatly affects the transient's response of the power supply. During the OFF period the inductor current charges the capacitor and causes the output voltage to increase, while during the ON period the capacitor provides the needed current for the load resistor causes the output voltage to decrease. Since the increase and decrease of the capacitor current is approximately linear, then the variation of the current has an average of $\Delta I_{out}/4$. The output voltage ripple (on the capacitor) equals to ($\Delta Q/C$) or (($\Delta I_{out}/4.T/2$)/C) [1]. Thus

$$C = \frac{\Delta Iout}{8.f.\Delta Vo} \text{------- (11)}$$

Operating current density is given by wire manufactures based on 1000 circular mils per ampere (c.m. /A). Practical design uses a current density below that number. Current density as low as 200 c.m. /A may be used safely. The wire size can be calculated from the multiplication of the peak current by the decided current density [1], [5].

Where μ_o is the free space permeability = $4\pi \times 10^{-7}$ H/m and $\mu_r = 1$ for air.

3.2. Computer Aided Design (CAD) Program

The flowchart of CAD program shown in Fig. 3. Determines the component values, the appropriate core and the number of primary and secondary turns and their wire size. The program has two important subprograms, one of them is concerned with the selection of the core and the second concerned with the wire size of the winding of the transformer. After the subprograms execution complete the results of them fed into the main program to complete the calculations. Minimum duty cycle (D_{min}), peak primary current (I_{pp}) and the value of the primary inductance of the transformer L calculated in second step. Next steps calculate number of primary and secondary turns and output filter capacitor. Also the program calculates the limiting factors which are the transistor and diodes selection are based upon such as maximum collector (forward) current, peak inverse voltage and minimum switching time. The converter may have multiple output by using multiple secondary winding which is one of the many advantages of flyback converter.

4. Simulation

The simulation process done for the Power Stage and control stage as described below.

4.1.Simulation of the Power Stage

Modeling and analysis of a dc-dc converter has been achieved through various small signal linearization techniques. The linearized models are limited only to analyze the small signal steady-state operation when the duty cycle signal can be regarded as a constant. However, in most applications, the converter is frequently subjected to large signal step line/load transients, subsequently varying the duty cycle ratio to maintain input-output regulation. Due to the time varying and switching nature of the system, it is impossible to deduce the large signal performances from the small signal linear models. The large signal behavior of the converters is most

conveniently studied by simulation methods [10]. It is clear that the power stage means that the power dc-dc converter. As there are three dc-dc converters, the simulation process is repeated three times on each converter in the same way; therefore, the simulation of one converter can be seen only. A flyback converter that is simulated is shown in Fig. (2), The converter operation is represented by a cyclic change of two power stage topologies within each switching cycle. Once is for the on-time interval as shown in Fig. (3), when the power switch is ON and the commutating diode is OFF, while the other as shown in Fig. (4), is for the off-time interval when the power switch is OFF and the diode is ON. These two time interval are modulated by the duty cycle controller in such a fashion that the out power always maintains a constant voltage level regardless of the change of the input voltage level or the load. Such converters can be characterized as nonlinear time-varying systems and have presented considerable difficulties in modeling and analysis. Furthermore, either by design intent or through light load operation, a steady state cycle invariably contains a third interval during which the inductor magneto motive force (MMF) vanishes.

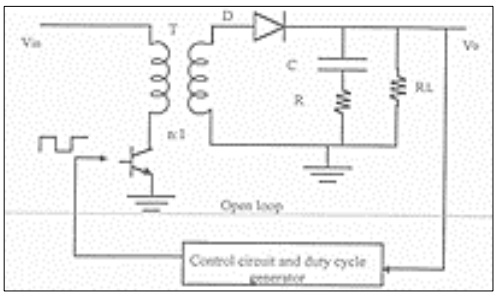

Fig. (2): Flyback dc-dc converter

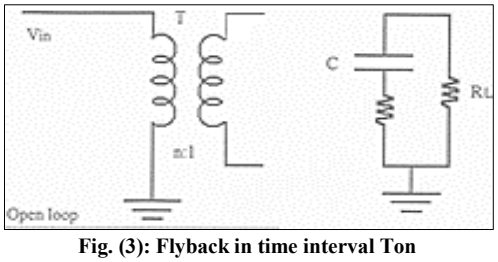

Fig. (3): Flyback in time interval Ton

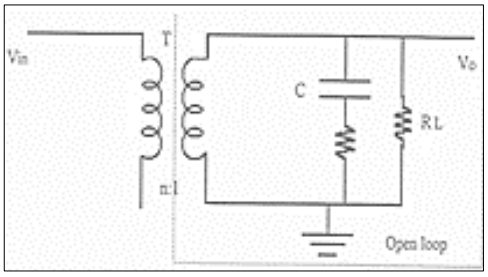

Fig. (4) Flyback in time interval Toff

During this time interval, both the power switch and the diode are in the OFF state [10]. As illustrated in Fig. (5), these time interval with the modes of operation help us to derive the required equations. The modes of operation are the continuous and discontinuous conduction. In continuous mode of operation, the current through the inductor is always greater than zero as shown in Fig. (6-a). The period of each switching cycle can be clearly divided into two time intervals, T_{on} and T_{off}. During T_{on} the power transistor is ON and the diode is OFF, and during T_{off} the power transistor is OFF and the diode is ON. In discontinuous mode of operation, the current through the inductor reduces to zero and resides at zero for a T_{off} time interval as shown in Fig. (6-b). In this T_{off} time interval both the transistor and the diode are OFF. The time intervals T_{on} and T_{off} defined in the continuous mode are valid in this mode. An integrated output voltage shown in Fig. (7), For large signal performance simulations, the mathematical model inevitably should include both continuous mode and discontinuous mod of operations. In addition, the model should also include certain nonlinearities such as power switch peak current protection circuit and the saturation effects of operational amplifiers which often play important roles in large signal transients [10].Also we must model the parts of the dc.-dc. Converter such as transistor, diodes, capacitor and the transformer. By the existence of the snubber circuit we can model the transistor by a switch with constant forward voltage drop and infinite reverse resistance, such as the diodes. The

capacitor is considered to be ideal by neglecting the effective series resistance of the capacitance which can be done practically by using more than one capacitor in parallel. For a practical transformer, the primary inductance is finite, and the winding has finite resistance. A current will flow in the primary circuit even when there is no load on the secondary circuit; this current is called the magnetizing current [5]. Since the ferrite material cores used in this

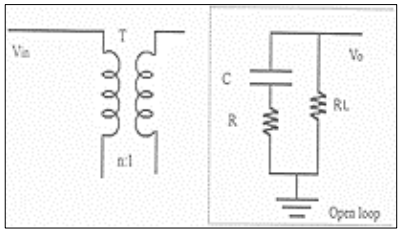

Fig. (5): Flyback in time interval Toff

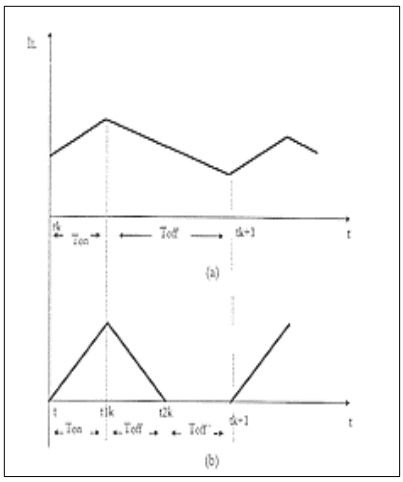

Fig. (6): Conduction modes with the time intervals

a) Continuous mode

b) Discontinuous mode

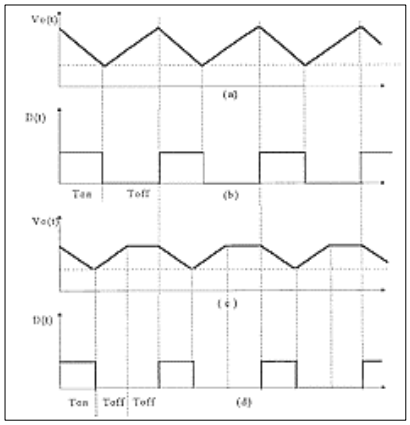

Fig. (7): Waveforms for integrated output Voltage and duty cycle signal
(a) And (b) for continuous mode operation
(c) And (d) for discontinuous mode operation

Conducting material, no eddy current loss is present. In the design we assume that the flux density to be at less than the half saturation density of the core then the area of the hysteresis is small which in turn reduces the losses due to hysteresis. Form the above the eddy current and hysteresis losses is small and then neglected [12, 13]. To simulate the flyback converter, we must model it mathematically with the following equations presenting each cycle of operation. For the case when the transistor is ON and the diode is OFF, the equations be:

$$I_L=V_{in}/r+ (I_{Lo}-V_{in}/r)*e^{-t.r/L}\text{------ (12)}$$

$$V_c=V_{co}*e^{-t.r/L}\text{------ (13)}$$

For K.T<t< (K+D).T

Where K is an integer K=0, 1, 2…

For the case when the transistor is OFF and the diode is ON the circuit description is:

$$I_L=-V_c/r+(I_{Lo}+V_c/r)*e^{-t.r/L}\text{------ (14)}$$

$$V_c=R*I_L+ (V_{co}-R*I_L)*e^{-t/R.C}\text{------ (15)}$$

For (K+D).T<t< (K+D+D1)

Where D1is the portion of the cycle when both the transistor and diode are OFF
Finally when the transistor is OFF and diode is OFF the circuit will have the following equation:

$$I_L=I_{Lo}\text{------- (16)}$$

$$V_c=V_{co}*e^{-t/R.C}\text{------ (17)}$$

For (K+D1).T<t< (K+1).T

The above equations can be solved at the end of their respective subintervals in terms of the state at the start of these subintervals. Give the initial conditions and a fixed duty ratio D; the equations are used to simulate the exact dynamic response of the circuit.

4.2.Simulation of the Control Stage

The control stage consists of analog multiplexer, analog to digital converter, the microprocessor and pulse width generator. The

most important part is the microprocessor, simulating the microprocessor mainly means simulating the operating program. Selection of new duty cycle is allocated by the system software implemented by the microprocessor. The software program compares the desired output with the actual one and decides a new duty cycle according to the difference between them and loads it in a binary number form to the counters which are represent the pulse width modulator correction the actual output voltage. The correction process is applied to the SMPS's respectively. The selection process of the output voltages of SMPS's with the correction process includes some small errors such as quantization error which concerned with the analog to digital converter and depending on the full scale reading of ADC.

4.3.Simulation Program

The first step in the simulation program is the initialization step. After initializing the duty cycle, solving the equations will be begun according to the time interval. At ON state equations (12) and (13) are solved until reaching to the OFF state, then the program solves equations (14) and (15).Also the simulation program tests if the operation mode is continuous or not by testing the inductor current. If the operation mode is discontinuous equations (16) and (17) will be solved. The simulation flowchart is shown in the Fig. (8).

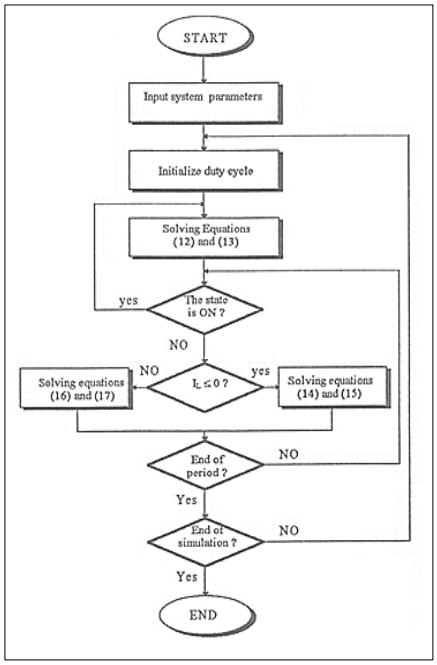

Fig. (8): Flowchart of simulation program

5. System Implementation

The practical Implementation of three switched mode power supplies controlled by one microprocessor contains the power stage and the control stages

5.1.Power Stage Circuits Implementation

5.1.1. Base Drive Circuit

Many base drive circuits may be used with the switched power supplies. Fig. (9), shows one of the simple base drive circuits which is used in this work. This base drive circuit consists of a transistor as a main part and resistors, this transistor connected as a buffer with inverted output. The advantages of this circuit are providing low source impedance with high current fed to the switching transistor leading to minimum saturation losses.

5.1.2. Protection Circuits

Many protection circuits provided in this stage. First of them is shown in Fig. (10), consist of the protective elements R,C and D which are connected in parallel with the primary winding of the transformer, the function of this circuit is to prevent voltage overshoot due to the unavoidable stray inductance when the transistor turns off. The other protection circuit is a snubber circuit; the whole protection circuit is shown in Fig. (11).

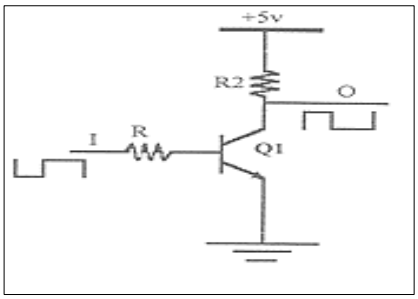

Fig. (9): Base drive circuit

5.1.3. CAD Results for the Power Converters

CAD program gives us the design of the power Converters by giving the values of the components and also suggesting suitable transistors and diodes which are convenient to the designer requirements to make it easier for the designer.

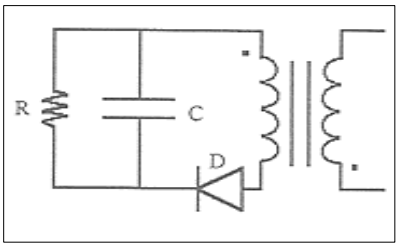

Fig. (10): Protection circuit

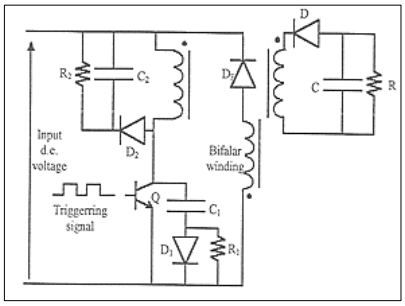

Fig. (11): Protection circuits with the flyback dc-dc converter

To understand the results, the input specification of each SMPS used in this paper is given in table (1). Table (2-a) and table (2-b) are the results of the CAD program. These specifications are the results of the sub program (routine) as mentioned in the Fig. 3. . The CAD program suggests using MJ10013 transistor which is a Darlington transistor with a speed up diode, also suggests using BYX71 fast recovery diode in the output rectifier and BYX55 the other diodes used in this paper. All these suggestions can be alternated by the designer according to the availability and the cost of these components considering the same specifications of all the components.

Table (1): the input specification of the three SMPS's.

The input specification of the three SMPS			
Input specification	SMPS-3	SMPS-2	SMPS-1
Input ac. voltage	90 – 150v	90 – 150v	90 – 150v
Operating switching frequency	23.4kHZ	23.4kHZ	23.4kHZ
Maximum duty cycle	0.45	0.45	0.45
Output voltage	-12V	12V	5V
Maximum ripple	0.06V	0.06V	0.025V
Maximum output power	6W	24W	20W
Maximum output current	0.5A	2A	4A

5.2.Control Stage Implementation

The control stage is a digital control system consists of the microprocessor with EPROM memory, digital pulse width modulator and system clock generator.

The control stage acts as the feedback path to close the loop of the converter. By comparing the output voltage with a desired reference voltage and accordingly changing the duty cycle that can alter the output voltage. Although many control techniques can be employed to implement a switched mode power supply control circuit, the fixed frequency-variable duty cycle is by far the most popular choice.

5.2.1. Microprocessor Controller Board

The hardware of 8085 microprocessor board is presented as shown in Fig.15. This includes the microprocessor chip with its standard bus architecture and peripheral components [14]. In general, a microprocessor system may include two types of memory devices: EPROM and RAM. Only EPROM memory is used in the

implemented system since it is not needed to replace the software program each time the whole system used and do not needed an interface card to do that. The IC2764 is used as an EPROM which has a capacity of 8KB, this memory is used to store the software program used by the microprocessor and also store the values of desired voltage of each SMPS since it is a fixed output. If the output variable, the desired voltage insets manually by dip switches to deal with it. The microprocessor executes many jobs; as mention some of them briefly in the following points:

- The microprocessor works as Selection port.
- Correcting the error happened in the Output of each SMPS.
- Synchronize the operation of all Peripheral IC's connected with.
- Works as a fault detector.

Table (2): the result of CAD program

a) The specification of the power dc – dc converter.
b) The specification of the converters transformer.

(2-a)

CAD results	SMPS-1	SMPS-2	SMPS-3
Maximum duty cycle	0.3299	0.3299	0.3299
Peak primary current	0.6837A	0.82A	0.205A
Primary inductor	3.656mh	3.0468mh	12.1875mh
No.of primary turns	156 turns	156 turns	254 turns
AWG of primary winding	28	27	33
No. of secondary turns	9 turns	19 turns	26 turns
AWG of secondary winding	21	24	26
Output capacitor	1.709mf	0.356mf	0.0887mf

(2-b)

Transformer specification	SMPS-1	SMPS-2	SMPS-3
Transformer type	UU 25/40/13	UU 25/40/13	UU 15/22/6
Air gap length	0.839mm	1.007mm	0.3965mm
Effective area	100 mm2	100 mm^2	30 mm2
Maximum flux density	0.16 T	0.16 T	0.16 T

5.2.2. Analog Multiplexer

The IC4052 as analog multiplexer with four inputs and one output which is enough for three SMPS are used, the analog multiplexer selects the output of SMPS will be regulated, this selection process is controlled by the microprocessor. The output of the power converter is fed to voltage divider before the analog multiplexer to be compiling with the analog to digital which followed the multiplexer. Certainly the ratio of the voltage divider differs from output to output of the converters to equal the maximum output voltage of each one to the full scale reading of ADC.

5.2.3. Analog to Digital Converter

The ZN427 analog to digital converter is used with a voltage reference equals to 2.5v and 8 bit output. To convert the analog voltage in synchronization with the digital system in the control stage and not to be confused, the ADC gives a signal from busy pin to the latch IC when the conversion process still in continuous. The ADC with the analog multiplexer represents an intermediate stage between the power stage and the control stage. Fig. 16.shows the circuit diagram of the ADC with analog multiplexer.

5.2.4. Variable Pulse Width Modulator

It is a simple digital circuit used to generate a pulse whose width is determined by the 8085 microprocessor. This circuit consists of an input latch, 8-bit binary up-down synchronous counter with clear. The digital circuit generates a pulse width modulated waveform at fixed carrier frequency of (23.400 kHz) which represents the switching frequency of the transistor. This clock signal is derived from the system clock generator (which will be discussed later). As we mentioned before the microprocessor sends a digital number consist of 8 bit to the PWM which is latched and then loaded to the counter when the counter finishes the previous counting operation, this number represents the binary value of the width of the pulse. It is important to notice that loading a FF

(Hexadecimal) number causes the maximum pulse width which is equal to the maximum allowable duty cycle of the switching frequency (i.e. it is equal to 45% of the duty cycle).

5.2.5. System Clock Generation

In the implemented system many clock frequencies which are synchronized to each other are needed. A crystal is used to generate a stable clock at a frequency of 12MHz. this high frequency clock is divided by 512via three counters to get the switching frequency which is equal to 23.4 kHz used in PWM. Also a 4MHz clock frequency is obtained by the same why which is used to clock the microprocessor.

5.3. Software Implementation Program

First of all, the microprocessor selects the actual output of the first SMPS in synchronous with its desired output to be compared and corrected, then selects the second one to have the same procession then the third SMPS , after that repeats this cycle from beginning and still scanning the three SMPS's. if there are any undesirable errors such as turning-off the main electric power, there is a reset switch to reset the operation of the whole system .To select the desired and the actual outputs instantaneously, the microprocessor sends a two digit number to the analog multiplexer to select the proper actual output and sends to the EPROM an address which represents the location of the desired output for the same SMPS in the same instant and latched them until they process. After the selection of the desired and actual outputs, the second steps begin. The microprocessor compares these two outputs and determined the error and then multiplies this error by a certain factor to get a digital number which loaded to the PWM to convert this number to a pulse with new width which used to turn the switching transistor ON with new duty cycle improving the actual output. To arrange the whole operations in the control stage, the synchronization between the control components are needed, that is done by giving output signals from the microprocessor to the other IC's to do their jobs such as reading from the memory, reading the output of the DAC and choosing the proper SMPS by the analog multiplexer, also a synchronization needed to determine the time needed by the SMPS's to change their output as the duty cycle changed and the whole time needed to change the width of the duty cycle, beginning from operation of the analog multiplexer, ADC, the microprocessor and PWM finally. At last the microprocessor detects any possible fault caused by any SMPS, this is necessary especially when there are multi-SMPS's. The main advantage of the fault detector is clearly appeared when one of the SMPS is not needed to work or a damage happened, so the whole system still work without turning it off but pointing to the damage part by lads representing each SMPS. Also any fault in the range of the main input voltage or any faults in the load leading to exceed the maximum rate of the output parameters which are the microprocessor detected and appeared in the lads.

Simulation and Experimental Results. The implemented circuit operation was tested and showed satisfactory capabilities, in terms of steady state and transient response. Simulation and the experimental results obtained from the prototype design.

The same thing when the load change from full load to half load, the increase in output voltage requires a new duty cycle to reduce it. Fig. (12), illustrate a step change from full load to half load. Fig. (13), illustrate the change in duty cycle versus output voltage for three SMPS's. The duty cycle alternates from minimum to maximum and the output changed according to that alternate.

All above mentions figures show slight differences between simulation result and experimental result that belongs to many reason such as quantization error which can be neglected and assuming ideal switching in the simulation program.

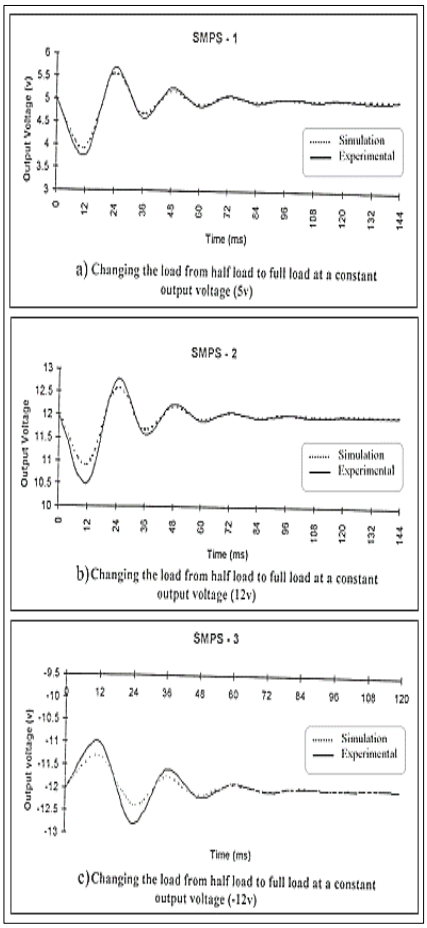

Fig. (12): Changing the load from half to full load for three SMPS's Simulation and experimental results.

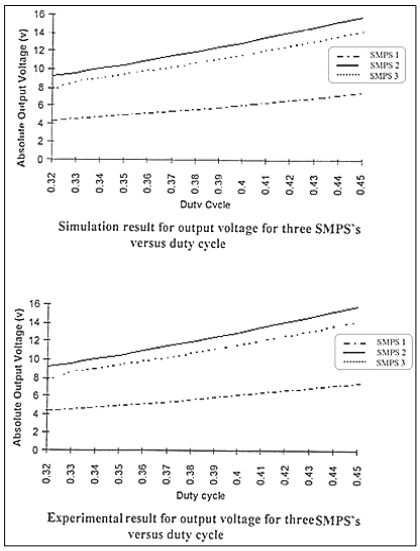

Fig. (13): Simulation and experimental results for output voltage for three SMPS's versus duty cycle.

6. Conclusions

In this paper, the one microprocessor is used to control the operation of three SMPS's with different output specification for each one. Using one microprocessor is so efficiently and easily. The features of the microprocessor lead to reduce the overall component count and increase the flexibility of the work. The overall time used to control three SMPS's is less than the processed speed; therefore a delay loop is used in the software implemented by microprocessor. The prototype can be used in control board in in a practical applications.

It is possible to use the control board in a central room while the SMPS's are placed in other rooms and scanning the operations of the these

SMPS's from a display screen placed with the control board or using microprocessor of a personal computer instead of the control board to do the same purposes, so in this case the monitor of the computer displays the behavior of the power supplies.

7. References

[1] George Chyrssis, "High-frequency switching power supplies: theory and design ", Mc Graw-Hill Book company, Network, 1984.

[2] E.S.Tez "An overview of microprocessor applications in power electronics and electrical drivers", University of Technology Loughborough, England 1985.

[3] Bryan Norris, "Microprocessors and microcomputers and switching mode power supplies", Mc Graw-Hill Book company, Network, 1978.

[4] John S. Contino and John R. Cielo "High-Converter for Power Supply Applications", Intermag conference, Koyoto, Japan, April 1972.

[5] Kader H.A. Al-Shara, Bassam M. J. Al-alousi "Design, simulation and implementation of microprocessor controlled Flyback Switched Mode Power Supply", College of Engineering Journal, Al- Nahrain university, Vol.4 (1) December, 2000.

[6] Nasir Coruh, Satilmis Urgun et al., "Design and Implementation of Flyback Converters", 5th IEEE Conf. on Industrial Electronics and Applications, pp.1189-1193, 2010.

[7] Daniel Hart, "Power Electronics",1st edition, McGraw Hill publications, 2011.

[8] Sanjeev Kumar Pandey, Dr. S.L.Patil, and Mrs. Vijaya S. Rajguru, "Isolated Flyback Converter Designing, Modeling and Suitable Control Strategies", Conf. on Advances in Power

Electronics and Instrumentation Engineering, PEIE,2014.

[9] Nagesha C, A. Sreedevi and Muniraj Gopal, "Simulation and hardware implementation of 24 watt multiple output Flyback converter", Power and Advanced Control Engineering (ICPACE), IEEE Conference, 2015.

[10] W. T. Almassy, K. B. Keller, and D. G. Nieraeth, "Designing microprocessor-based supervisory and control circuits for system power supplies", Mullett Associate, Inc., Los Angeles, CA, 1986.

[11] O.Ojo "Robust control of series parallel resonant converters", IEE Proc. Control theory appl. Vol. 142, No.3, September 1995.

[12] Fred C. Y. Lee, and Yuan Yu, "Computer-aided analysis and simulation of switched d.c. to d.c. converters" , IEEE transactions on industry applications, Vol. IA – 15, No. 5, September/October 1979.

[13] Philips data handbook, Electronic component and material, ferroxcube for power, audio/video and accelerators, part 5, March 1982.

[14] R. Gaonkar, "Microprocessor architecture, programming & applications with the 8085/8080 A, second edition, Merrill Publishing Co., USA, 1989.